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PRIORITY DOCUMENT

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I HEREBY CERTIFY that annexed hereto is a true copy of documents filed in connection with the following patent application:

Application No.	S990361
Date of Filing	30 April, 1999
Applicant	SUPERGOLD TECHNOLOGY LIMITED, a Cypriot Company of c/o Optimal Systems Limited, Molesworth House, 1 South Frederick Street, Dublin 2, Ireland.

Dated this 15TH day of May, 2000.

An officer authorised by the
Controller of Patents, Designs and Trademarks.

FORM NO. 1

Request for the Grant of a Patent S990361

PATENTS ACT, 1992

The Applicant(s) named herein hereby request(s)

☐ the grant of a patent under Part II of the Act

☒ the grant of a short-term patent under Part III of the Act

on the basis of the information furnished hereunder

1. **Applicant(s)**

Name: SUPERGOLD TECHNOLOGY LIMITED

Address: c/o Optimal Systems Limited,
Molesworth House,
1 South Frederick Street,
Dublin 2,
Ireland

Description/Nationality: A Cypriot Company

2. **Title of Invention:** **DATA COMMUNICATION**

3. **Declaration of Priority on basis of previously filed application(s) for same invention (Sections 25 & 26)**

Previous Filing Date	Country in or for which Filed	Filing No.

4. **Identification of Inventor(s)**

Name(s) of person(s) believed by Applicant(s) to be the Inventor(s)

Names(s):	Timothy O'Farrell, a United Kingdom citizen	Ahmed Al-Dabbagh, a United Kingdom citizen
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5. **Statement of right to be granted a patent (Section 17(2)(b))** S 990361

The applicant is the assignee of the inventors by virtue of a Deed of Assignment dated 14th April 1999.

6. **Items accompanying this Request - tick as appropriate**

(i) ☒ prescribed filing fee (£50.00)
(ii) ☐ specification containing a description and claims
☒ specification containing a description only
☒ drawings referred to in description or claims
(iii) ☐ an abstract
(iv) ☐ copy of previous application(s) whose priority is claimed
(v) ☐ translation of previous application whose priority is claimed
(vi) ☒ Authorisation of Agent (this may be given at 8 if this Request is signed by the Applicant(s)

7. **Divisional Application(s)**

The following information is applicable to the present application which is made under Section 24:-

Earlier Application No. ..... Filing Date .....

8. **Agent**

The following is authorised to act as agent in all proceedings in connection with the obtaining of a patent to which this request relates and in relation to any patent granted:-

MACLACHLAN & DONALDSON, 47 Merrion Square, Dublin 2

9. **Address for Service (if different to that at 8)**

MACLACHLAN & DONALDSON, at their address as recorded for the time being in the Register of Patent Agents (Rule 92)

Signed Name(s) SUPERGOLD TECHNOLOGY LIMITED

By ...J. M. McKeown.....
MACLACHLAN & DONALDSON, Applicants' Agents

Date: 30th April 1999

DATA COMMUNICATION

The present invention relates to data communication and more particularly, to data communication using spread spectrum techniques. The invention also relates to communication applications using signature sequences.

Spread spectrum communication techniques are used for information carrying signals in a variety of communication systems because of their ability to reduce the effects of certain transmission impairments. Many multi-user communication techniques suffer co-channel interference, multiple access interference and intersymbol interference. The use of spread spectrum transmission and reception attenuates these interference types.

In Local Area Networks (LANs) there is an increasing need for wireless access. This wireless access allows mobile computer users to remain in contact with a given corporate LAN over short distances. Currently available systems provide such connections using either radio or infrared communication technology. For certain system requirements, this communication is adequate. However, the data transmission rates achievable are relatively low and this significantly limits the number of applications to which the systems may be applied and implementation costs are often prohibitive.

Wireless local area network (WLAN) products were thus for a long time a specialty, made available by a small number of vendors and built according to meet proprietary requirements. The Institute for Electrical and Electronic Engineers (IEEE) in June 1997 formalized a standard that will control interoperability of such products known as 802.11. While this standard will undoubtedly promote the growth of WLAN products, the problems of transmission rates, reliability and cost remain. One possible solution is obtained by the application of spread spectrum communication techniques using signature sequences. While implementations of this type overcome the traditional problems, it is difficult to synchronise data communication without the use of complex circuitry. Synchronisation difficulties include symbol synchronisation, chip synchronisation and signal strength measurements (SSM) as well as the problem of synchronisation maintenance.

One solution to these problems has been proposed by Haris for use used in the new 802.11 WLAN standard at 11 Mb/s. In common with most proposed solution there is an acquisition phase and a maintenance phase. Acquisition in this case, is accomplished using a single correlator and an embedded Barker sequence. Synchronisation is maintained using an early-late detector. While the previously know 'Harris type' transition detector solution is practical in a wide variety of applications, the early-late detector operates directly on the incoming sequence stream, which is composed of modified Walsh codes at the input. This leads to reliability problems in that quality of the signal cannot be guaranteed.

There is therefore a need for a method and apparatus, which will overcome the aforementioned problems.

It is an object of this invention to provide a method and apparatus for data communication which delivers synchronisation acquisition in terms of chip and symbol synchronisation and signal strength measurement.

It is a further object of the invention to provide synchronisation maintenance in terms of chip synchronisation.

It is a still further object of this invention to allow compatibility to synchronise across the various modes of communication.

Accordingly there is provided a method and apparatus for data communication in a WLAN network using M-ary signaling.

Preferably M-ary signaling is used for synchronisation of data communication in the network.

Preferably the synchronisation scheme utilises Supergold structured codes for acquisition.

Ideally, the synchronisation scheme also utilises Supergold structured codes for maintenance.

In one arrangement maintenance is achieved using an early-late detector.

In a particularly preferred arrangement, synchronisation signals are derived at the output of a correlator bank during data detection wherein the incoming sequence stream incorporates structured codes as mentioned above. This provides a significant improvement in reliability in synchronisation resulting from an improved signal. This implementation allows for the codes to be used for all aspects of communication reducing circuit complexity and cost as well as component count and possibility for error during fabrication of data communication networks. Furthermore, the data communication method and apparatus are more resilient to noise as a result of implementation after correlation.

Preferably, the sum of the responses of all correlators to the repetitive periodic transmission of one code, is a constant.

Preferably, the difference between the sum of the responses of the odd-group correlators and the sum of the responses of the even-group correlators or *vice versa,* defines a periodic bipolar waveform.

In a preferred embodiment, the periodic bipolar waveform is a square waveform.

Preferably, a transition detector circuit is used at the correlator outputs deriving substantial signal to noise ratio benefit from the processing gain advantage of spread spectrum.

Ideally, the waveform has a period equaling half the chip rate.

Preferably, the correlator coefficients are configured such that when one sample is taken per chip with all signals and correlation taken to be in bipolar form that the sum of the responses of all correlators to the repetitive periodic transmission of one code, is a constant

Ideally also the difference between the sum of the responses of the odd-group correlators and the sum of the responses of the even-group correlators or *vice versa,* is a periodic bipolar waveform with a period equaling half the chip rate. Both of these properties being particularly useful for synchronisation acquisition purposes. Preferably, the difference is a square waveform.

Ideally, both the method and apparatus described above are formed for both acquisition and maintenance of synchronisation.

Ideally, a transceiver of the system is formed that implements the concept of acquire-and-maintain.

Preferably, a threshold value is determined in response to an operational mode governing the link.

In one arrangement the threshold may be lowered to half of the peak height if the mid-samples are discarded. This later approach requires a further *gating logic* to block the mid-samples from being passed onto the threshold circuitry

Preferably the symbol acquisition circuitry will deliver a periodic *single* pulse with a periodicity equaling the symbol period.

Ideally, the time epoch of the pulse coincides with the *peak* sample in the upper waveform.

The invention will now be described more particularly with reference to the accompanying drawings, which show, by way of example only, one embodiment of data communication method and apparatus according to the invention. In the drawings:

Figure 1 shows a codebook used in synchronisation schemes of the invention;
Figure 2 shows a correlators bank for use in the invention;
Figure 3 shows packet synchronisation;
Figure 4 shows a tapped delay line correlator;

Figure 5 shows sum(0,2) and sum(1,3);

Figure 6 shows symbol-synchronisation acquisition;

Figure 7 shows operation of a symbol synchronisation acquisition scheme;

Figure 8 shows symbol synchronisation declaration;

Figure 9 shows a Harris type transition detector;

Figure 10 shows a sampling-dependant clock;

Figure 11 shows a modified version of the Harris type transition detector of Figure 9.

Figure 12 shows a chip synchronisation detector;

Figure 13 shows output of a Supergold chip synchroniser under perfect and imperfect input waveform sampling;

Figure 14 shows signal strength measurement unit;

Figure 15 shows instantaneous signal strength;

Figure 16 shows the three elements of acquisition;

Figure 17 shows symbol synchronisation loss detection;

Figure 18 shows mode ir(1);

Figure 19 shows synchronisation for mode ir(1);

Figure 20 shows symbol synchronisation (normalised waveforms);

Figure 21 shows output of chip synchroniser under perfect and imperfect input waveform sampling;

Figure 22 shows instantaneous signal strength measurement;

Figure 23 shows output of chip synchroniser under perfect and imperfect input waveform sampling;

Figure 24 shows instantaneous signal strength measurement;

Figure 25 shows mode ir(2);

Figure 26 shows symbol synchronisation (normalised waveforms);

Figure 27 shows symbol synchronisation (normalised waveforms);

Figure 28 shows instantaneous ssm (perfect synchronisation condition);

Figure 29 shows output of chip synchroniser under perfect and imperfect input waveform sampling: I-channel;

Figure 30 shows output of chip synchroniser under perfect and imperfect input waveform sampling: Q-channel;

Figure 31 shows mode ir(3);

Figure 32 shows symbol synchronisation (normalised waveforms);

Figure 33 shows instantaneous signal strength measurement;

Figure 34 shows output of chip synchroniser under perfect and imperfect input waveform sampling: I-channel;

Figure 35 shows output of chip synchroniser under perfect and imperfect input waveform sampling: Q-channel; and

Figure 36 shows mode ir(4).

For the purposes of this specification reference will be made to the codebook of Figure 1 used in the synchronisation method and apparatus of the invention. The codebook is used to set each of the coefficients of a bank of correlators for use in the invention shown in Figure2.

For convention, the first code, S_0, is selected for periodic application to the input of the bank of correlators. The sum of the response of the 0^{th} and 2^{nd} correlators, denoted by Sum(0,2) (for the purposes of this specification the convention Sum(i,j) will be used to denote the summation of the i^{th} and j^{th} correlator outputs.), is an ideal impulse occurring at twice the symbol rate. Additionally, the sum of the outputs of the 1^{st} and 3^{rd} correlators, Sum(1,3), has the same property but is time-delayed by ¼ of a symbol period. The table shown below gives the profile and the relationship between the two summations, where the peak value of 16 has been normalised to unity.

Sum(O,2)	1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0
Sum(1,3)	0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0

In addition use of the codebook in setting correlator coefficients in this way ensures that, providing one sample is taken per chip with all signals and correlation taken to be in bipolar form that:-

the sum of the responses of all correlators to the repetitive periodic transmission of one code, is a constant; and

the difference between the sum of the responses of the odd-group correlators and the sum of the responses of the even-group correlators or *vice versa* is a periodic bipolar square waveform with a period equaling half the chip rate.

Both of these properties being particularly useful for synchronisation acquisition purposes :

There are two elements to synchronisation in data communication, irrespective of data type, namely, the acquisition and maintenance of synchronisation.

Acquisition is carried out at the start of data transmission and its sole purpose is to acquire the incoming signal by aligning the receiver chip and symbol clocks with the incoming signal.

Maintenance techniques are used to maintain the chip and symbol clocks in line with the incoming signal during the transmission of the data.

Ideally, the receiver must be in synchronisation all the time with the transmitter. Consequently, synchronisation *maintenance* techniques are used to maintain both the chip and symbol clocks in line with the incoming signal. However, the availability of synchronisation related information for synchronisation updates may not be present all the time in the receiver. Hence, synchronisation maintenance techniques often adjusts synchronisation when possible, otherwise the receiver is made to flywheel.

For Synchronisation a simple protocol is imposed on the transceiver operation that basically implements the concept of acquire-and-maintain. The 802.11 standard packet format, which has been adopted by the Harris/prism chip set, follows this concept. The protocol outline is shown in Figure 3.

No data is transmitted during the header section of the transmission. Both chip and symbol synchronisation and the signal strength are determined during this acquisition phase. Other aspects of synchronisation acquisition may be performed during this period.

Synchronisation which includes frequency and phase estimation, such as in RF systems does not form part of the current invention and is omitted for clarity.

In the data section, the receiver makes synchronisation updates when synchronisation related information becomes available from the samples of the received signal e.g. chip/symbol transitions. Alternatively the receiver is made to "flywheel", when such information is not derivable from the samples of the received signal.

For chip synchronisation to be possible, two samples per chip are needed, thereby doubling the sampling rate. Thus the correlator is designed to have double the length of the delay line of the correlator to 32. From a detection point of view, the number of taps, however, may be kept at 16, where in this case, a tap is drawn from every other position in the delay-line. The correlator design is shown in more detail in Figure 4 but this does not compromise the adopted synchronisation algorithms.

A perfect periodic impulse being obtained from the sum of the 0^{th} and the 1^{st} correlator output while transmitting code S_0 periodically ensures that the resultant zero sidelobe of the summed correlation occurs because of the relationship between code S_0 and code S_2. This is also true for S_4, S_6, S_8, S_{10} etc. Since this periodic impulse is at twice the symbol rate, some form of 'frequency halving' must be employed which removes the ambiguity in the symbol synchronisation point. For example, taking the odd peaks to correspond to the alignment of one complete received code, S_0, within the delay line of the 0^{th} correlator, the even peaks may be taken to correspond to the natural response of the 2^{nd} correlator to the code S_0. In this context, this translates to an inherent discrepancy as to which of the peaks of Sum(0,2) corresponds to the correct timing edge. Given that, say, the odd peaks occur when the received S_0 resides completely inside the 0^{th} correlator delay-line; and the fact that the codes themselves are orthogonal, then at each odd/even peak epoch of the Sum(0,2), a decision can be made whether the peaks correspond to the correct timing edge or not, on the basis of the output of the correlators $Corr(S_0)$ and $Corr(S_2)$. If the output of the 0^{th} correlator is greater than the output of the 2^{nd} then the peak corresponds to the correct timing edge.

Figure 5 shows the summing of Corr(S_0) and Corr(S_2) and the summing of Corr(S_1) and Corr(S_3) in response to the periodic transmission of code S_0. The former and latter are marked with *'s and o's respectively. Figure 6 shows the implementation of the symbol synchronisation acquisition scheme, where it is assumed that code S_0 is periodically transmitted. The summation of correlators Corr(S_0) and Corr(S_2) is used as inputs to a thresholding circuit, which uses a pre-specified threshold. The outputs of the correlators of interest are also applied to a comparison logic which, when strobed, determines if the output of Corr(S_0) is greater than Corr(S_2).

Every time Sum(0,2) passes the threshold, a comparison is made between the output Corr(S_0) and Corr(S_2). If the output of Corr(S_0) is greater than Corr(S_2), then a symbol synchronisation is declared by driving the output of the comparison logic high; otherwise the output is made low.

It is clear from the results of Figure 5 that the threshold of Figure 6 must be chosen carefully and its value may very well be affected by which communication mode the link is operating in.

When the symbol S_0 is applied periodically, and Corr(S_0) and Corr(S_2) outputs are applied to the comparison circuit and Sum(0,2) is fed to the input of the threshold. Here, it suffice to use a threshold of height ¾ of the peak sample value to detect the time epoch of the peak sample and suppressing all the others. The threshold may be lowered to half of the peak height if the mid-samples are discarded. This later approach requires a further *gating logic* to block the mid-samples from being passed onto the threshold circuitry. Such gating logic will in one arrangement use the derived chip clock. The later approach will increase the probability of correct synchronisation, resulting in less probability of missed data. This preferred solution illustrates the reason that flywheeling is not being used.

The upper waveform in Figure 7 constitutes the Sum(0,2), which is applied to the thresholding circuit. After the thresholding and comparison, the output obtained from the comparison circuitry is shown as the lower waveform in Figure 7. It can clearly be seen that the symbol acquisition circuitry of Figure 6 will deliver an ideal periodic *single* pulse

with a periodicity equaling the symbol period. Moreover, the time epoch of the pulse coincides with the *peak* sample in the upper waveform.

During the acquisition phase, symbol synchronisation is declared with a high degree of certainty after the successful acquisition of several contiguous symbols. A symbol synchronisation assessment circuit is therefore needed to track the output of the symbol synchronisation acquisition of Figure 6, and declare if the symbol timing has been successfully acquired with sufficient certainty. One such circuit is shown in Figure 8.

Here, a counter, which counts a pre-defined number of sampling clock pulses, is initialised on the occurrence of the *first* symbol pulse emerging from the symbol synchronisation acquisition circuitry. The counter's all-zero state is detected and an add-and-accumulate circuit is used to count the number of times the counter all-zero state coincides with the presence of a pulse in the output of the symbol synchronisation acquisition circuitry. Symbol synchronisation is declared when the accumulator contents exceed a constant pre-specified value, C out of L symbols.

The Harris chip set (described in brief above) takes two samples per chip. Ideally, a sample is required to be placed in the middle of one chip. The other sample will fall in the mid point between the mid samples of the two consecutive chips, i.e. on the chip transition in the case when there is a chip transition. Chip synchronisation adjustment can only be made when a chip transition occurs and is detected.

When a chip transition takes place then, with two samples per chip the following sample patterns shown in Figure 9 are possible. The two *end* samples shown in the figure are used for correlation, the mid and end samples are used for synchronisation purposes. The procedure is as follows:

1 Determine if a chip transition has occurred. A chip transition occurs when the two *end* samples have different signs. The chip transition flag is set.

2 If chip transition occurs then determine if a chip synchronisation error occurred. This is done by comparing the sign of the *mid* sample with the

signs of the two *end* samples.

3 If the sign of the *mid* sample is the same as the RHS sample, then sampling is speeded up (Late flag is set). Else sampling is slowed down (Early flag is set).

Note this technique will always make a synchronisation adjustment when there is a chip transition. The logic required for the Harris chip tracking is also shown in Figure 9.

Three outputs are produced. The chip transition flag (F) indicates that chip synchronisation information is available when driven to logic '1'. When set, the early (E) and late (L) flags indicate that the sampling clock is early and late, respectively.

The difference between the sum of the responses of the odd-group correlators and the sum of the responses of the even-group correlators is a periodic square waveform with a period equaling half the chip period. This is the case when the sampling is perfect, i.e. one sample lies in the middle of the chip while the other lies on a chip transition. The middle plot of Figure 10 depicts this case.

The effect of early, perfect and late sampling on the resultant periodic square waveform is also given in Figure 10. The early and late conditions can be seen from the two plots by noting the start of the waveform in each plot. The three shown waveforms constitute the different clock profiles obtained in response to the periodic transmission of code S_0, where two samples per chip were taken and the correlators are based on Figure 4.

While when the sampling is perfect, samples fall at the maximum (+16) and the minimum (-16), whilst other samples fall exactly at the middle point between the two waveform extremes indicating the usefulness of a circuit based on the Harris type transition detector can be used, this circuit is used at the correlator outputs and therefore, derives substantial signal to noise ratio benefit associated with the processing gain advantage of spread spectrum.

Figure 11 shows a modified version of the Harris type transition detector of Figure 9. The modification is required because it is desired to derive chip synchronisation using the signal available in Figure 2, which is no longer binary in general.

The addition of a thresholding logic, denoted by T in the diagram, essentially converts the potentially non-binary clock of Figure 2, into a three-level waveform. Consider the third sample (Smp(3)), which can take a value between -16 and +16. The value of Smp(3) is represented in sign (one bit, a_1) and magnitude (multiple bits, b_1) format and are applied to the level discrimination circuit confined within the shaded box in the figure. The outputs of the level discrimination circuit are the sign bit a_2 and the flag bit b_2. The thresholding circuit denoted by T, gives a logical '1' if its input is greater than the threshold level 'T' and zero otherwise. The overall action of the level discriminator is described by the truth table below.

Input Range	a_1	b_1	a_2	b_2	Equivalent Decimal Representation of a_2, b_2.
$ip \geq +T$	0	> h	0	1	1
$0 < ip < +T$	0	< h	0	0	0
$-T < ip < 0$	1	< h	0	0	0
$ip \leq -T$	1	> h	1	1	-1

The above described level discrimination circuit is applied to the other two samples, Smp(1) and Smp(2), in the delay line to derive their respective (a_2,b_2) values. The outputs (a_2,b_2) from all the three samples are employed as inputs to a series of adders. The threshold circuit T is used to determine the synchronisation status (E, L and F), that implements the function shown in the following function.

$$T(ip) = \begin{cases} 1 & if\ |ip| > 0 \\ 0 & otherwise \end{cases}$$

For the waveforms of Figure 10, the 4 possible scenarios of the sample distribution for the early, late and perfect sampling conditions are described in the tables below, for a

threshold value of T=8. Note, scenario 1 and 2 correspond to the high-to-low and low-to-high chip transitions, respectively.

	Perfect Scenario 1		
	Smp(1)	Smp(2)	Smp(3)
	+16	0	-16
(a_2,b_2)	+1	0	-1
Adders	+2	+1	+1
F	+1		
E		+1	
L			+1

	Perfect Scenario 2		
Smp(1)	Smp(2)	Smp(3)	
-16	0	+16	
-1	0	+1	
-2	-1	-1	
+1			
	+1		
		+1	

	Early Scenario		
	Smp(1)	Smp(2)	Smp(3)
	+16	+16	-16
(a_2,b_2)	+1	+1	-1
Adders	+2	0	+1
F	+1		
E		0	
L			+1

	Late Scenario		
Smp(1)	Smp(2)	Smp(3)	
-16	+16	+16	
-1	+1	+1	
-2	-2	0	
+1			
	+1		
		0	

A new chip synchronisation module forming part of the invention is shown in Figure 12. The clock obtained from processing the output of the bank of correlators is input directly to the modified transition detector. The outputs of the transition detector are then used to affect the sampling of the input waveform to the bank of correlators.

In Figure 13, three plots are given which show the effect of prefect and imperfect sampling of the input waveform to the bank of correlators upon the outputs of the chip synchronisation status detector.

It is important to note that the transiton detector described above implements the chip synchronisation tracker of Figure 5 before correlation, that is to say at chip level. For this reason, such detectors specify that a *positive* signal-to-noise ratio is required in the chip bandwidth limiting the proposed solution. In contrast, the technique of the invention while similar to the traditional detector in concept, is implemented after correlation and does not require this restriction on the SNR ratio in the chip bandwidth, and thus has a broader dynamic SNR range of operation.

The sum of the responses of all the correlators (see above) was indicated as being constant at +16. Whereas, this constant value constitutes an instantaneous measure of the received signal strength and can be used to derive any signal-strength dependant threshold that is used in the receiver, e.g. the threshold required by symbol synchronisation acquisition (Figure 6) and chip synchronisation status detector (Figure 12).

This signal strength measurement continues to give the required results when the two samples per chip are taken with the correlators as shown in Figure 4. Furthermore, it is also valid under all perfect and imperfect chip synchronisation. However due to the presence of additive noise, it is recommended to average the instantaneous signal strength measure over a number of symbols.

A simple method for implementing an averaging process is to use an add-and-accumulate circuit. The instantaneous signal measure is fed to an adder, which adds this measure to an accumulated sum. The adder output is stored in an accumulator, whose output is fed back to the adder. This process of addition, accumulation and feedback is carried out at the sampling rate. Every 2*N samples, the contents of the accumulator are clocked to a register and the content of the accumulator is cleared. As a result, the register will hold a measure of the average signal strength taken over N symbols. Figure 14 shows the structure of the signal strength measurement unit.

Figure 15 gives a plot of the instantaneous signal value obtained from the summation of all outputs from the bank of correlators. This was generated taking two samples per chip and under perfect sampling scenario.

Both symbol and chip synchronisation acquisition units employ a threshold in order to derive their respective outputs. This threshold is dependent on the signal strength and hence can be derived from the SSM unit of Figure 14, whose output is required to be scaled appropriately in order for the symbol and chip synchronisation acquisition units to operate correctly. Figure 16 shows how the three acquisition elements may coexist in the

final synchronisation architecture. The two scaling factors shown in the diagram may not be equal and depend on the communication mode of operation.

Once the acquisition phase is completed, the receiver then switches to data receiving mode. During this phase, the receiver must remain in synchronisation in order for optimum data detection to be possible.

The exact symbol timing epoch having been determined from the symbol acquisition phase of the transmission, a counter mechanism is then used to periodically activate the data decision circuit and hence produce received estimates of the transmitted data. Such a counter mechanism gives a symbol synchronisation condition once every 32 samples (one symbol period). In fact the counter, which counts upto-32 sampling clock pulses of Figure 8, constitutes the counter mechanism for this purpose. Once initialised and symbol synchronisation is declared, then one complete symbol can be assumed to be resident in the bank of correlators whenever the counter reaches the all-zero state.

Symbol synchronisation loss detection, however, is still required to declare such an event when it occurs. One way to implement such a detector is shown in Figure 17.

The bank of correlators outputs are fed into a selector circuit, which uses the detector output as the address of the correlator number to process. The selected correlator output is then thresholded to determine if it has fallen below a pre-defined level, denoted by V. The threshold circuitry produces a +1 if the input is above the threshold V, otherwise 0 is produced; that is

$$V_v(ip) = \begin{cases} 1 & \text{if } ip \geq v \\ 0 & \text{otherwise} \end{cases}$$

The threshold circuitry output is applied to an add-and-accumulate circuit, which will count the number of times the detected correlator output is above the threshold V. On the application of a start monitoring instruction, a counter counts up to K at the symbol rate. On the detection of the all-zero state, the content of the accumulator is examined. If the

value contained in the accumulator is below a pre-specified value, D, then symbol synchronisation loss state is declared. Hence this detector design will give a symbol synchronisation loss declaration when the selected correlator output has fallen D out of K times below the threshold, V.

The chip synchronisation acquisition circuitry of Figure 16 can also be used for chip synchronisation maintenance, where in the acquisition phase, the received signal is assumed to be resulting from the periodic transmission of one pre-specified symbol. In the case of synchronisation maintenance, the received signal will be due to the random transmission of symbols. This added randomness will affect the way the synchronisation tracker is implemented for different communication modes of operation.

During the data-receiving mode, the signal strength estimate will vary in the presence of different symbols in the received signal. Whether this is the case or not can very well depend on the communication mode the system is operating in. However, this is not a problem. A simple protocol solution can be implemented which will over come this problem. In such a solution the obtained signal strength measurement from the synchronisation acquisition mode is assumed to be also valid during the data receiving mode and hence, no further signal strength measurement is considered in the later mode. The averaging of the signal strength measurement during the transmission of random data will be further investigated in the future. In developing an appropriate averaging technique, the receiver can be made more adaptive to instantaneous signal strength variation during the transmission of random data.

In the Mode IR(1) : Half-Rate mode, the upper and lower codebooks are identical and are constructed from the Supergold codes by selecting the first 8 codes from the original 16-by-16 codebook. The target 16-by-16 codebook, C_I, is then constructed from the selected 8 codes and their complement giving a total of 16. C_I is then used in the upper and lower branches of the transceiver as shown in Figure 18. It will be assumed that the receiver is AC coupled.

Since only half of the original codebook is used, this scheme differs from that of Figure 16 in the following:

At the transmitter, only half of the original codebook is used. The other half is totally ignored.
At the receiver, only half of the correlators are need.

The above means that half of the structure of Figure 16 is now missing. In particular, Sum(3) and Sum(4) are no longer available and can be considered to be zero in the context of Figure 16.

Since effectively, the same waveforms are obtained from the upper and lower banks of 8-correlators, two options for connecting the synchronisation scheme emerge.

The first is to apply Sum(1) and Sum(2) to the synchronisation unit of Figure16 and zeroing the inputs Sum(3) and Sum(4). Hence this option uses, say, the Rx upper branch for the purpose of synchronisation, and this is shown in Figure19.

The second option is to sum the corresponding Sum(1) and Sum(2) from the Rx upper and lower correlator banks and then feed then into the synchronisation unit, in a similar manner to that of the first option.

During the synchronisation acquisition phase, one symbol, which is known to both the transmitter and receiver, is transmitted periodically.

Figure 20 shows the obtained correlation waveforms due to the periodic transmission of code S_0. It is clear from the figure that the waveforms possess the required properties, shown in Figure 5, which are needed for symbol synchronisation acquisition. The symbol synchronisation section of the synchronisation acquisition module of Figure 16, will therefore still be applicable here.

Figure 21 shows the obtained chip synchronisation results due to the periodic transmission of code S_0 and for the three possible synchronisation conditions. The threshold in Figure 12 was set to +2. This threshold is adequate for the noiseless case. However, it will have to be set at a higher level when additive noise is considered.

The above results clearly show that the signaling structure of this mode, has no detrimental effect on the chip synchronisation section of the synchronisation acquisition module of Figure 16, and is therefore still applicable here.

Figure 22 shows the obtained SSM results due to the periodic transmission of code S_0 and for the three possible synchronisation conditions. Here, the obtained estimate is not continuously constant. However, the summation of any 16 samples and subsequent division by 8 will always give 16. This is true for any of the three synchronisation conditions.

When compared with the instantaneous measurement of Figure15, it is clear that the above waveforms appear to have suffered a 50% loss of signal. This can be attributed to the fact that only half of the original codebook is used as discussed in section 0.

Figure 23 shows the obtained chip synchronisation results due to the random transmission of all the codes and for the three possible synchronisation conditions. The threshold of Figure 12 was set to +8.

The above show that randomising the transmitted symbols combined with raising the threshold of Figure 12 to +8, allows the chip synchronisation section of the synchronisation acquisition module of Figure 16 to be still applicable during the data section of transmission.

Figure 24 shows the obtained SSM results due to the random transmission of all the codes and for the perfect synchronisation conditions. Here, the obtained estimate is not continuously constant as in the ideal case of Figure 15. Furthermore, it appears that there is not any simple and straightforward procedure for extracting the estimate of the signal

strength. This suggests that SSM should be carried out during the synchronisation acquisition phase and the estimate obtained is used during the data phase of the packet.

In the Mode IR(2) : Half-Rate mode, the upper and lower codebooks are not identical. The target codebooks for the upper and lower branches of the system, C_I and C_Q, respectively, are constructed using exactly the same procedure for mode IR(1), with C_Q being constructed from the lower half of the original Supergold codebook. See Figure 25.

Again, note the transmitter sends out the unipolar versions of C_I and C_Q; the transmitted code members from C_I and C_Q are effectively algebraically added during transmission through the optical channel. The correlator's coefficients in the Rx are all bipolar. It will be assumed that the Rx is AC coupled.

Due to the structure of this mode, both the upper and lower banks of 8-correlators at the receiver will experience codes from the upper and lower codebooks in the transmitter. Since C_I and C_Q are different, the corresponding outputs of the two banks of correlators will also be different, two options for connecting the synchronisation scheme emerge. The first is to use only the upper bank of correlators for synchronisation in an identical manner to that of Figure 18. The second option is to apply a second synchronisation unit (Figure 16) to the outputs of the lower bank of correlators and thus obtain another set of synchronisation flags. In this case, the synchronisation information from the upper and lower synchronisation units will have to be combined together by OR-ing corresponding outputs from the upper and lower synchronisation units. While the first approach offers less complexity, the second method is expected to give an increase in the synchronisation update rate and hence reliability.

Ideally, the corresponding first codes from C_I and C_Q would be transmitted periodically during the acquisition phase of the transmission. However, and due to the structure of the received signal and the two correlator banks, the output of the bank of correlators used for symbol synchronisation no longer maintain the same profile as that shown in Figure 20.

Figure 26 shows the correlation waveforms obtained from the 1st group of correlators in response to the periodic transmission of the corresponding first codes from C_I and C_Q, simultaneously.

It is evident from these waveforms that the circuit of Figure 16 will fail to achieve the required initial symbol synchronisation, without some modification.

Two solutions to this problem are possible. The *first approach* is a protocol solution and that is to constrain the periodically transmitted symbol to one code from C_I. No code from C_Q will be transmitted during this phase of the transmission. As a result, this will effectively produce the same correlation in the receiver as those obtain for IR(1), and hence the same synchronisation procedure will be applicable here too.
The *second approach* is to transmit the corresponding codes from C_I and C_Q, but in this case, the outputs of the 1st and 2nd correlators are added together to give an impulsive clock, which is used to clock the thresholding circuit. The waveform upon which the synchronisation is made, is derived by subtracting the output of the 3rd correlator from the output of the 1st correlator. Figure 27 shows the correlation waveforms obtained.

When waveform 1 is active, the threshold circuit Figure 16 produces a '1' if waveform 2 is above a pre-specified threshold or '0' if below the threshold. The correct symbol timing is derived by counting the appropriate number of samples forward (or backward) so as to align the periodically received symbol within the delay line of the corresponding correlator.

While the first solution complements the synchronisation schemes for the previous modes, the second solution reduces the complexity of the synchronisation protocol.

The chip synchronisation is not affected by the use of either approach given above. The value for the threshold in Figure 12 can be set to 2 or higher.

SSM can be obtained by the summation of the two threshold estimates obtained from the upper and lower synchronisers, see Figure 28. This solution is also chip-sampling independent.

Figures 29 and Figure 30 show the obtained chip synchronisation results due to the random transmission of all the codes and for the three possible synchronisation conditions. The threshold in Figure 12 was set to +8. Signal strength measurement in this case is the same as described above for mode IR(1).

Mode IR(3) : Half-Rate (Differential)

In the Mode IR(3) : Half-Rate (Differential) mode, the upper and lower codebooks are not identical. The target bipolar codebook for the upper branch of the system, C_I, is constructed using exactly the same procedure for mode IR(1). The target bipolar codebook for the lower branch of the system, C_Q, is derived from the lower half of the original Supergold codes. See Figure 31.

Again, note the transmitter sends out the unipolar versions of C_I and C_Q; the transmitted code members from C_I and C_Q are effectively algebraically added during transmission through the optical channel. The correlator's coefficients in the Rx are all bipolar. It will be assumed that the receiver is AC coupled.

This mode is very much similar to IR(2) in the sense that both the upper and lower banks of 8-correlators at the receiver will experience codes from the upper and lower codebooks of the transmitter. This is again due to the structure of the signaling of this mode. Hence, the same two solutions discussed for IR(2) will also be applicable here.

Figure 32 shows the correlation waveforms obtained for the purpose of symbol synchronisation from the periodic transmission of the corresponding first codes from C_I and C_Q.

It is evident from these waveforms that the circuit of Figure 16 will perform correctly to achieve the required initial symbol synchronisation. The outputs of the 0^{th} and 2^{nd}

correlators are added together to give an impulsive clock, which is used to trigger the thresholding circuit in Figure 16. The 0^{th} and 2^{nd} correlators outputs are then compared to derive the required symbol synchronisation.

With a threshold of +8, the chip synchronisation detector of Figure 12 will work correctly. Lowering the threshold to +4, leaves the operation of the early and late flags intact under imperfect chip synchronisation. However, with the later threshold value , the early and late flags alternately pulse, when the chip synchronisation is perfect; and their average alternating pulsing averages to zero.

SSM measurements for this mode is similar to that of IR(1). Figure 33 shows the obtained SSM results due to the periodic transmission of code S_0 and under perfect chip synchronisation conditions. Here, the obtained estimate is not continuously constant. However, the average taken over any successive 4 samples and subsequent scaling by a constant can always be made to give 16. This is true for any of the three chip synchronisation conditions.

Figures 34 and 35 show the obtained chip synchronisation results due to the random transmission of all the codes and for the three possible synchronisation conditions. The threshold in Figure 12 was set to +4. SSM will be identical to that described for mode IR(1).

In the Mode IR(4) : Full-Rate mode, the target upper and lower codebooks are not identical and they are identical to the target codebooks of mode IR(2) See Figure 36 . Again, the transmitter sends out the unipolar versions of C_I and C_Q; the transmitted code members from C_I and C_Q are effectively algebraically added during transmission through the optical channel. The correlator's coefficients in the receiver are all bipolar. It will be assumed that the receiver is AC coupled.

Due to the identical signaiing structure of this mode with that of IR(2), the same synchronisation methods, which are applicable to IR(2), will equally be valid for this mode as well.

Unlike optical systems, the RF platform naturally makes full use of the bipolar code signaling. Consequently, the Supergold codebook of Figure 1 and their relevant properties, which are described above, are directly applicable to the RF implementations. Since the synchronisation module of Figure 16 was developed using the relevant bipolar properties of the Supergold codes, it can be stated that the synchronisation module of Figure 16 constitutes the synchronisation module for the RF platform.

It will be understood that the current invention relates both to the specific architectures described as embodiments of the underlying invention namely the use of communication codes for synchronisation. This use has the technical effect of reducing component count, complexity and cost. Additionally the manner of use of the signal downstream of the correlators to improve signal quality and therefore system robustness is also an important feature of the invention. Both of the above being read in conjunction with benefits of using Supergold structured codes for this purpose.

It will also be understood that the method and apparatus described may be used in any suitable communication medium

It will be noted that the method and apparatus is not limited to implementation with the packet based IEEE 802.11 standard but may equally be implented for synchronous transmission with embedded synchronisation symbols.

It will of course be understood that the present invention is not limited to the specific details described herein, which are given by way of example only and that various modifications and alterations are possible within the scope of the invention.

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Applicants' Agents
47 Merrion Square
Dublin 2

Figure 1

Subset 0	Symbol No
+++-++--++-+++---	S_0
++-++++-+---+-++	S_1
+-+++---+++-++-+	S_2
+---+-+++-++++-	S_3
Subset 1	
+++-++-+-+---+++	S_4
++-++++--+++-+--	S_5
-+---++++++-++-+	S_6
-+++-+--+-++++-	S_7
Subset 2	
+++---+-+-++-+++	S_8
--+-+++--++++-++	S_9
+-++-+++++---+-	S_{10}
-++++-++--+-+++-	S_{11}
Subset 3	
---+++-++-++-+++	S_{12}
++-+---+-++++-++	S_{13}
+-++-+++---+++-+	S_{14}
-++++-++++-+---+	S_{15}

Figure 2

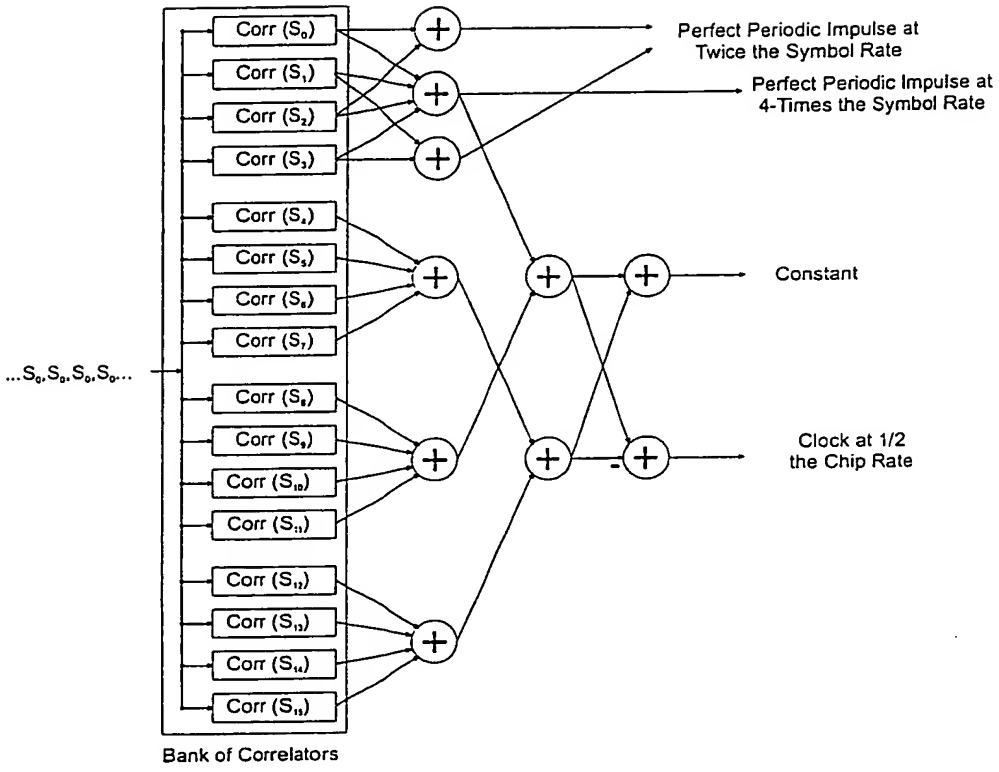

Corr (S_0)
Corr (S_1)
Corr (S_2)
Corr (S_3)
Corr (S_4)
Corr (S_5)
Corr (S_6)
Corr (S_7)
Corr (S_8)
Corr (S_9)
Corr (S_{10})
Corr (S_{11})
Corr (S_{12})
Corr (S_{13})
Corr (S_{14})
Corr (S_{15})
...S_0,S_0,S_0,S_0...
Bank of Correlators
Perfect Periodic Impulse at Twice the Symbol Rate
Perfect Periodic Impulse at 4-Times the Symbol Rate
Constant
Clock at 1/2 the Chip Rate

Figure 3

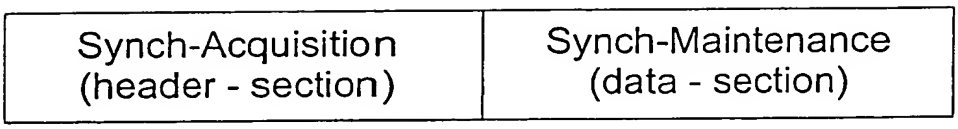
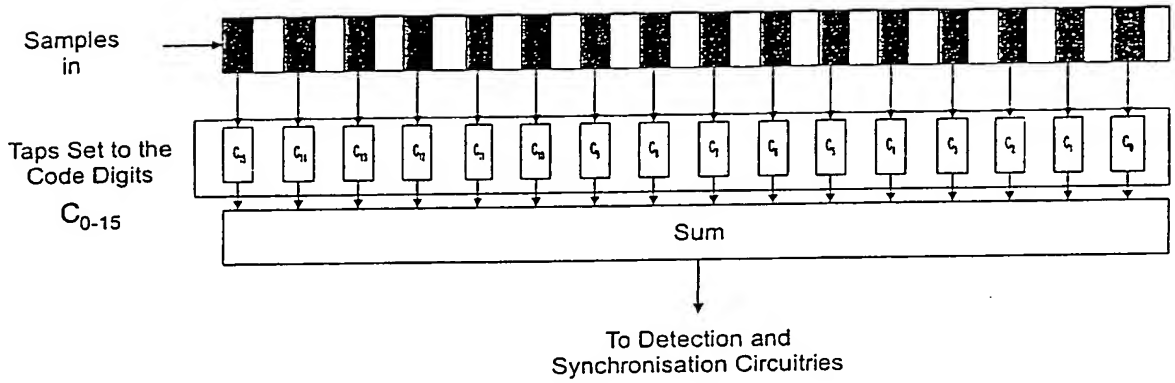

Synch-Acquisition
(header - section)
Synch-Maintenance
(data - section)

Figure 4


Samples in
Taps Set to the Code Digits
C_{0-15}
Sum
To Detection and Synchronisation Circuitries

5/35

Figure 5

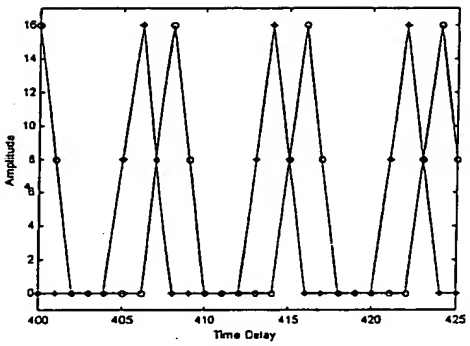


Figure 1: Sum(0,2) and Sum(1,3).

Figure 6

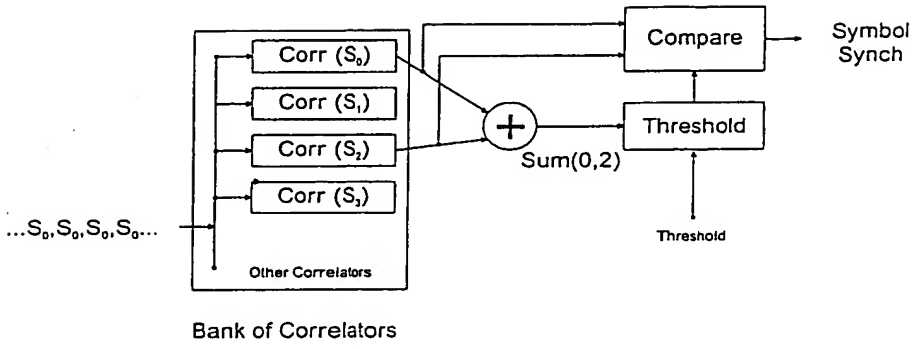

Compare
Symbol Synch
Corr (S_0)
Corr (S_1)
Corr (S_2)
Corr (S_3)
Threshold
Sum(0,2)
...S_0,S_0,S_0,S_0...
Threshold
Other Correlators
Bank of Correlators

Figure 7

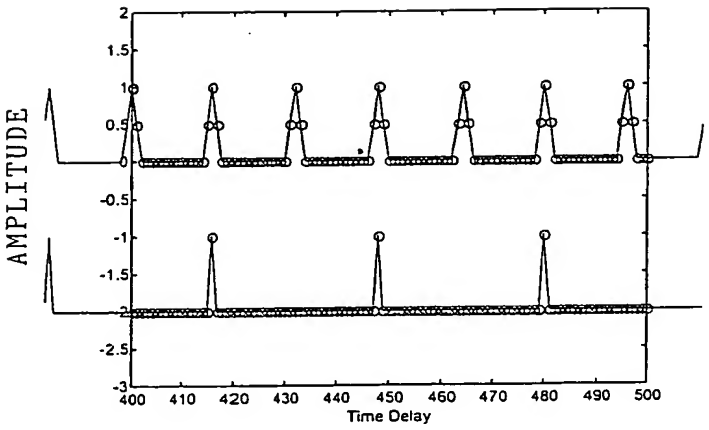

AMPLITUDE
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
-2.5
-3
400
410
420
430
440
450
460
470
480
490
500
Time Delay

Figure 8

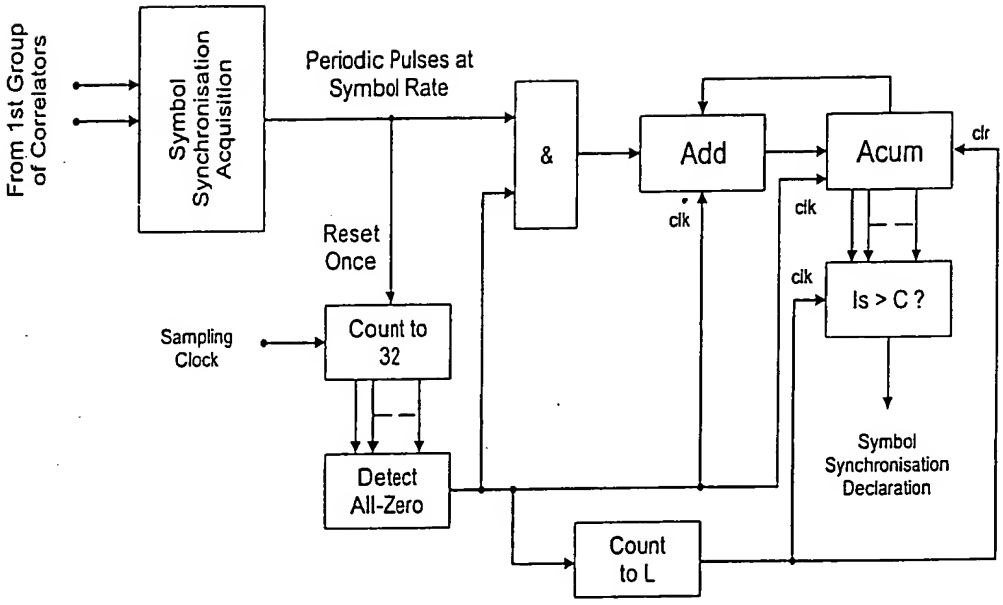
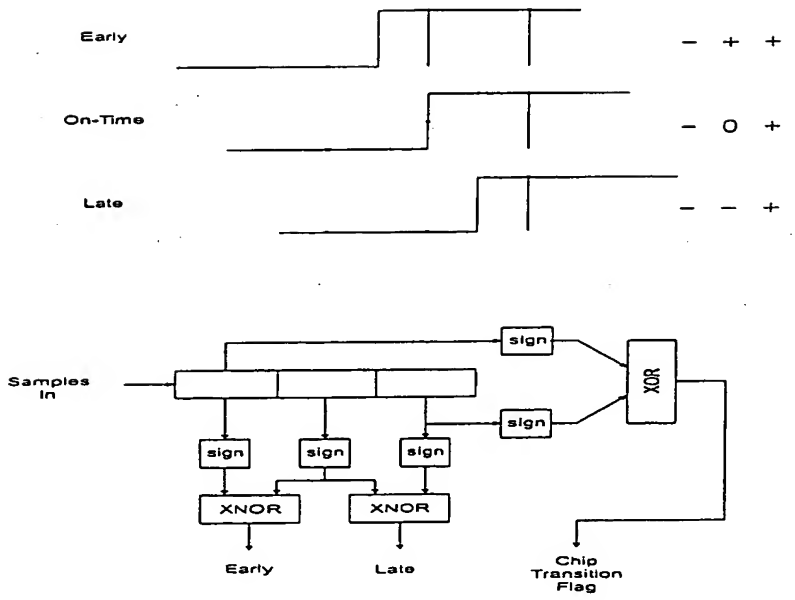

From 1st Group of Correlators
Symbol Synchronisation Acquisition
Periodic Pulses at Symbol Rate
&
Add
Acum
clr
clk
clk
clk
Reset Once
Sampling Clock
Count to 32
Is > C ?
Detect All-Zero
Count to L
Symbol Synchronisation Declaration

Figure 9


Early
On-Time
Late
– + +
– 0 +
– – +
Samples In
sign
sign
sign
sign
sign
XOR
XNOR
XNOR
Early
Late
Chip Transition Flag

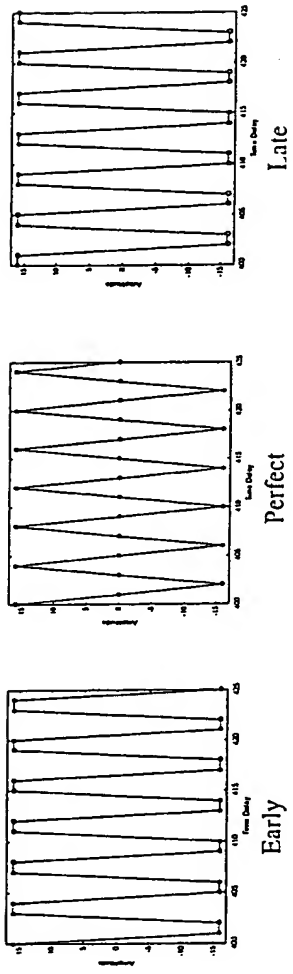


Figure 10

Figure 11

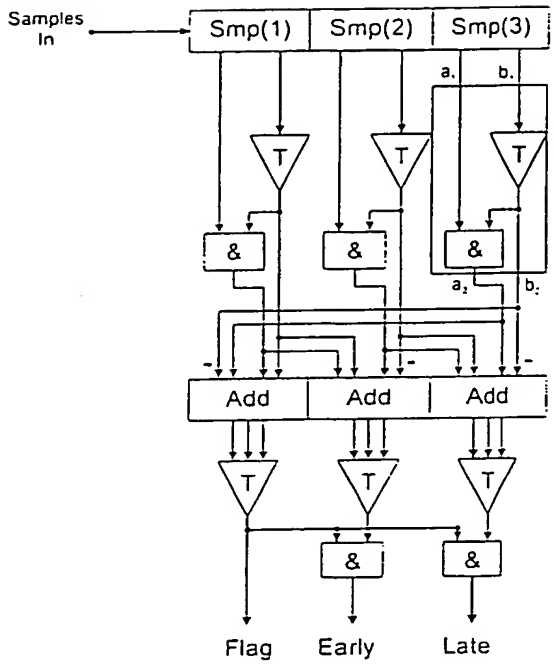


Figure 12

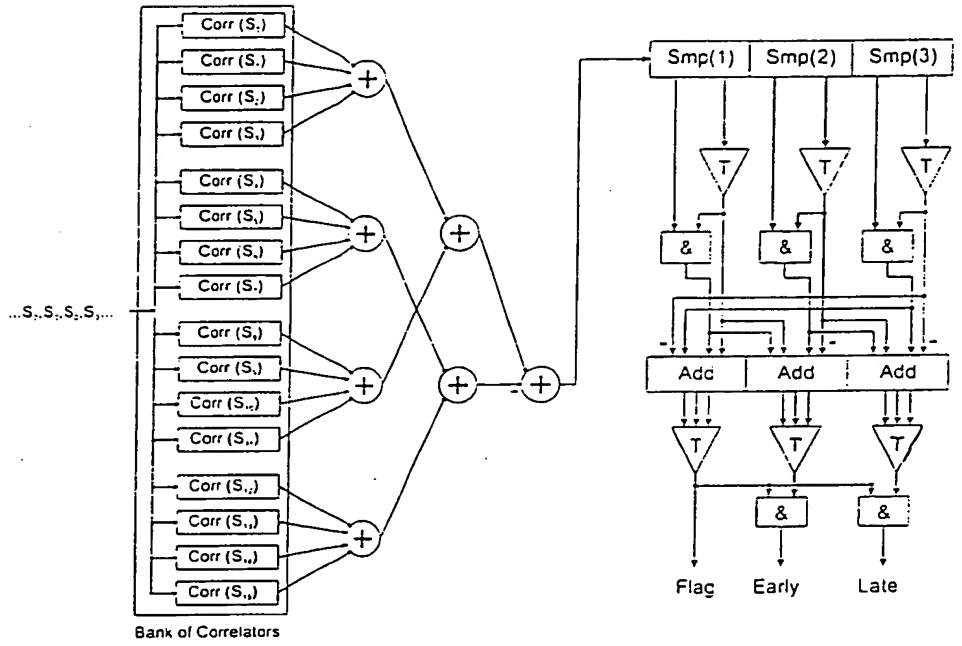
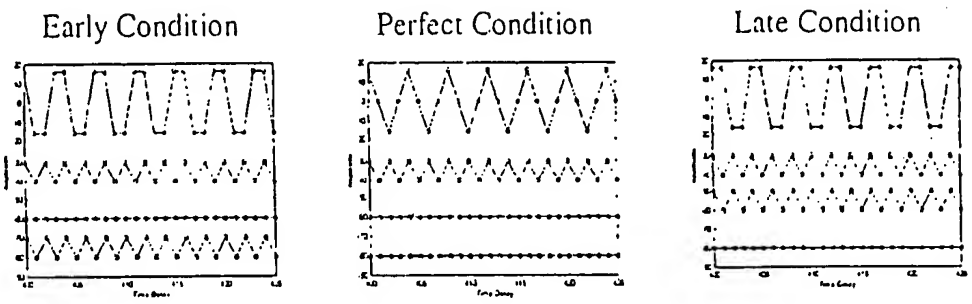

Corr (S-1)
Corr (S0)
Corr (S1)
Corr (S2)
Corr (S3)
Corr (S4)
Corr (S5)
Corr (S6)
Corr (S7)
Corr (S8)
Corr (S9)
Corr (S10)
Corr (S11)
Corr (S12)
Corr (S13)
Corr (S14)
...S-1,S0,S1,S2,S3,...
Bank of Correlators
Smp(1)
Smp(2)
Smp(3)
T
&
Add
Flag
Early
Late

Figure 13



Waveform 1 : The input to the synchronisation detector.
Waveform 2 : The synchronisation status flag.
Waveform 3 : The late flag.
Waveform 4 : The early flag.

Figure 14

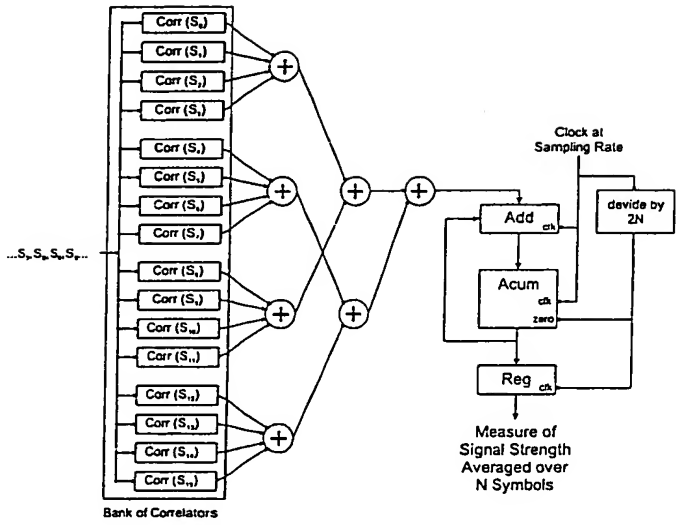

Corr (S0)
Corr (S1)
Corr (S2)
Corr (S3)
Corr (S4)
Corr (S5)
Corr (S6)
Corr (S7)
Corr (S8)
Corr (S9)
Corr (S10)
Corr (S11)
Corr (S12)
Corr (S13)
Corr (S14)
Corr (S15)
...S2,S1,S0,S-1,S-2...
Bank of Correlators
Clock at Sampling Rate
Add
clk
devide by 2N
Acum
clk
zero
Reg
clk
Measure of Signal Strength Averaged over N Symbols

Figure 15

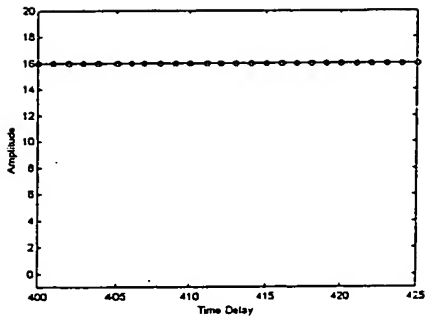

20
18
16
14
12
10
8
6
4
2
0
Amplitude
400
405
410
415
420
425
Time Delay

Figure 16

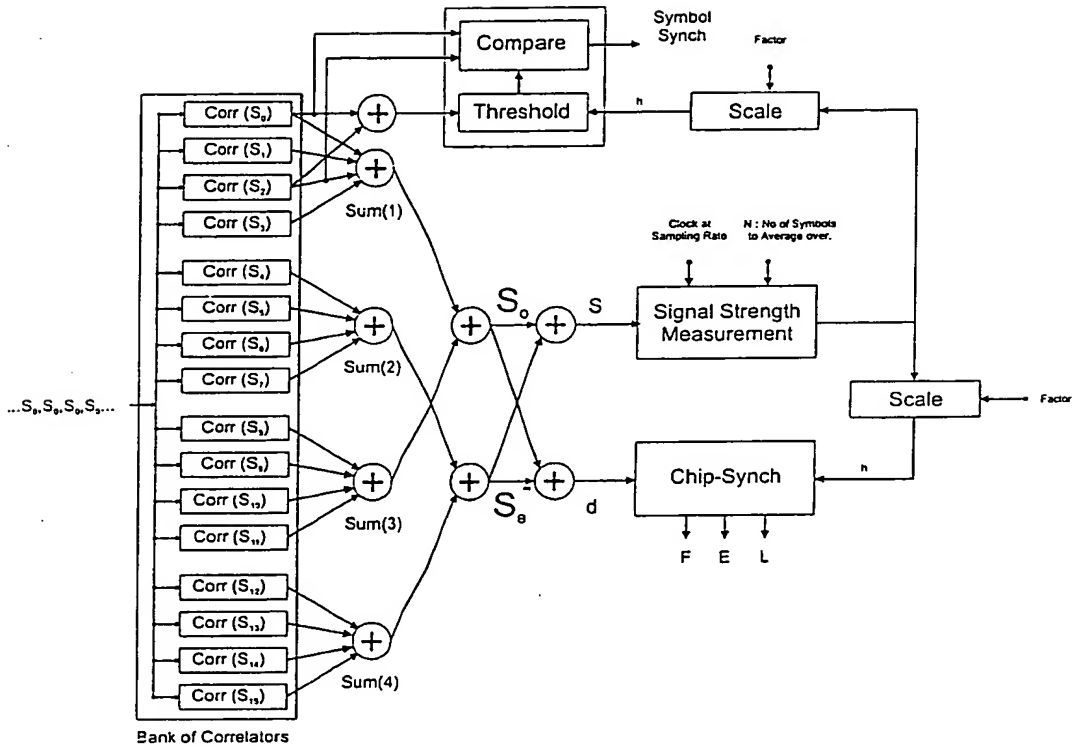

Compare
Symbol Synch
Factor
Threshold
h
Scale
Corr (S0)
Corr (S1)
Corr (S2)
Corr (S3)
Corr (S4)
Corr (S5)
Corr (S6)
Corr (S7)
Corr (S8)
Corr (S9)
Corr (S10)
Corr (S11)
Corr (S12)
Corr (S13)
Corr (S14)
Corr (S15)
Sum(1)
Sum(2)
Sum(3)
Sum(4)
Bank of Correlators
...S8,S9,S0,S1,S2...
Clock at Sampling Rate
N : No of Symbols to Average over.
So
Se
S
d
Signal Strength Measurement
Scale
Factor
Chip-Synch
h
F
E
L

Figure 17

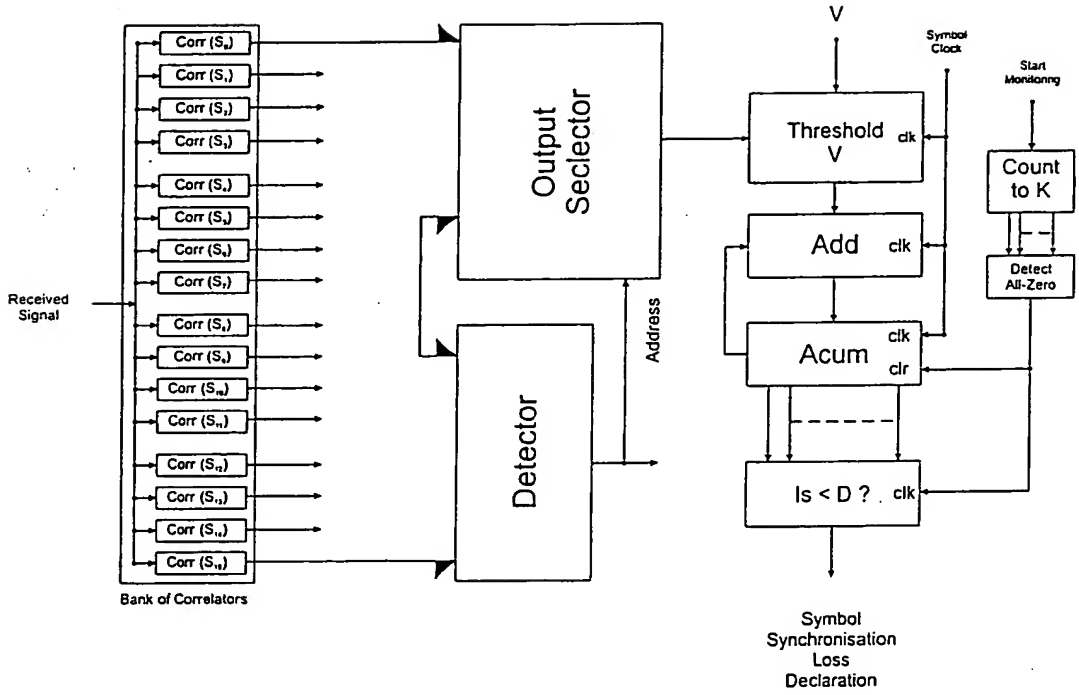

Received Signal
Corr (S_0)
Corr (S_1)
Corr (S_2)
Corr (S_3)
Corr (S_4)
Corr (S_5)
Corr (S_6)
Corr (S_7)
Corr (S_8)
Corr (S_9)
Corr (S_{10})
Corr (S_{11})
Corr (S_{12})
Corr (S_{13})
Corr (S_{14})
Corr (S_{15})
Bank of Correlators
Output Seclector
Detector
Address
V
Symbol Clock
Start Monitoring
Threshold V
clk
Add
clk
Acum
clk
clr
Is < D ?
clk
Count to K
Detect All-Zero
Symbol Synchronisation Loss Declaration

Figure 18

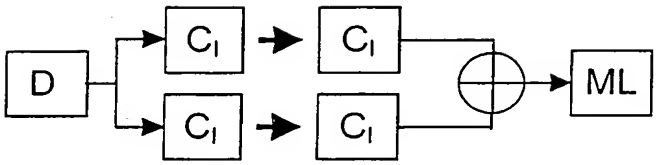


Figure 19

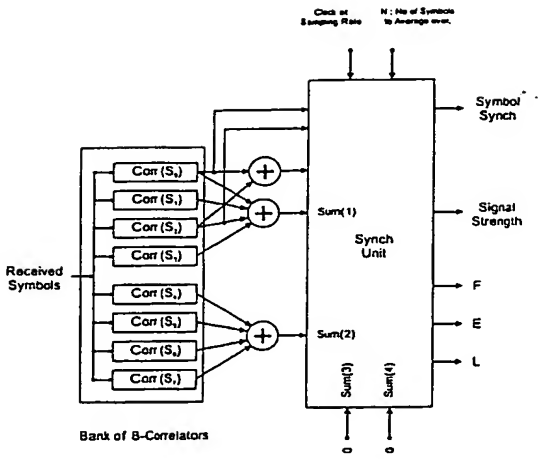
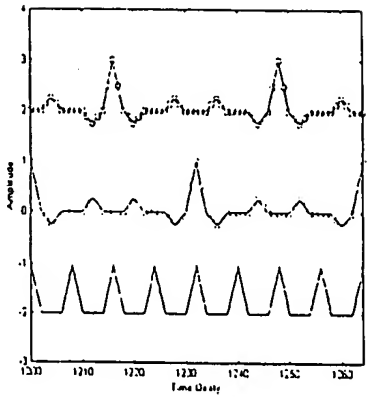

Symbol Synch
Signal Strength
F
E
L
Synch Unit
Sum(1)
Sum(2)
Sum(3)
Sum(4)
Received Symbols
Bank of 8-Correlators

Figure 20

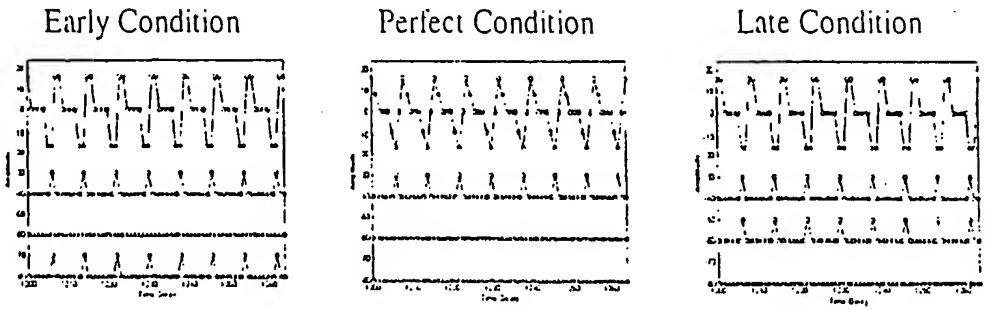


Waveform 1 : The correlation between the received signal and S_0. The signal peak at the value of +16 and its sidelobes vary about the zero axis.

Waveform 2 : The correlation between the received signal and S_3. This waveform is a time-shifted version of waveform 1.

Waveform 3 : Sum of waveform 1 and 2. This is a perfect impulse whose peak takes the value of +16.

Figure 21



Waveform 1 : Sum of S_e and S_o in Figure 16, which constitutes the input to the modified transition detector.

Waveform 2 : The transition detection flag (F).

Waveform 3 : The synchronisation-late flag (L).

Waveform 4 : The synchronisation-early flag (E).

Figure 22

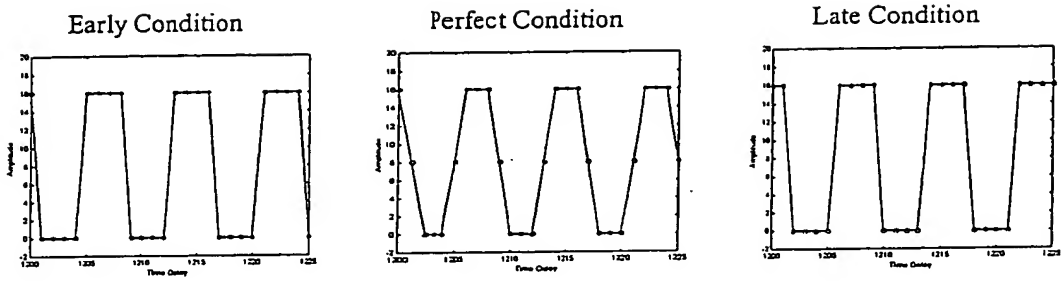
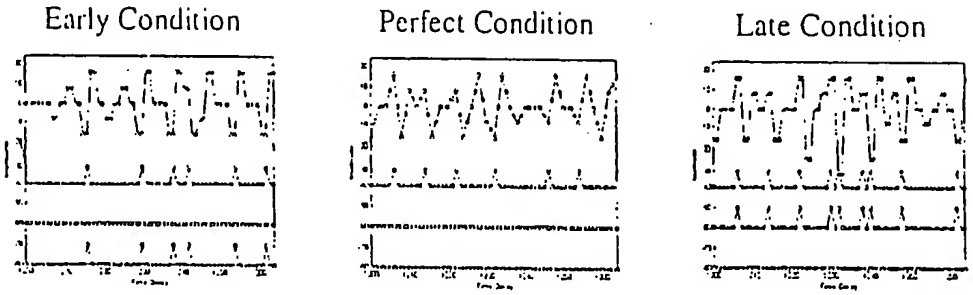


Figure 23



Waveform 1 : Sum of Sum(1) and Sum(2). This is the waveform, which constitutes the input to the modified transition detector.

Waveform 2 : The transition detection flag (F).

Waveform 3 : The synchronisation-late flag (L).

Waveform 4 : The synchronisation-early flag (E).

Figure 24

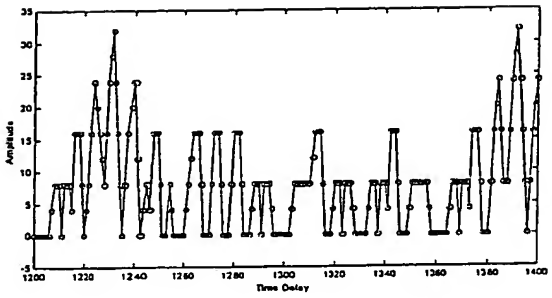

Amplitude
Time Delay
35
30
25
20
15
10
5
0
-5
1200
1220
1240
1260
1280
1300
1320
1340
1360
1380
1400

Figure 25

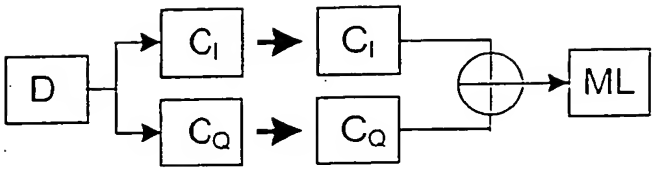
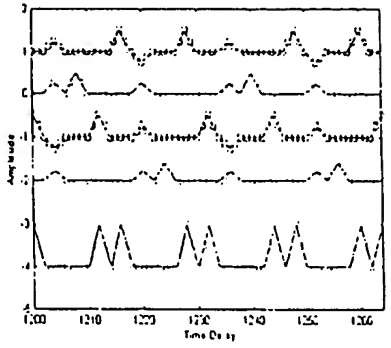
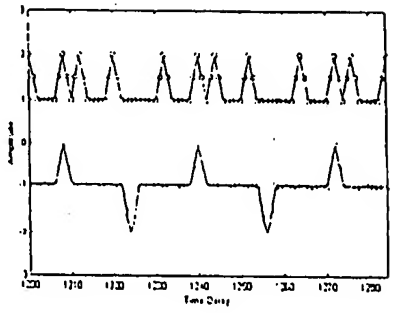


Figure 26



Waveform 1 : The correlation between the received signal and S_0.
Waveform 2 : The correlation between the received signal and S_1.
Waveform 3 : The correlation between the received signal and S_2.
Waveform 4 : The correlation between the received signal and S_3.
Waveform 5 : Sum of waveform 1 and 3.

Figure 27



Waveform 1 : The sum of the 1st and the 2nd waveforms.
Waveform 2 : The subtraction of the 3rd waveform from the 1st waveform.

Figure 28

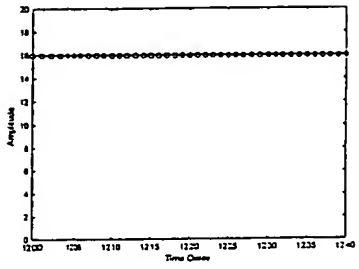

Amplitude
0
2
4
6
8
10
12
14
16
18
20
1200
1205
1210
1215
1220
1225
1230
1235
1240

Figure 29

Waveform 1 : Sum of S_e and S_o of Figure 16, which constitutes the input to the modified transition detector.
Waveform 2 : The transition detection flag (F).
Waveform 3 : The synchronisation-late flag (L).
Waveform 4 : The synchronisation-early flag (E).

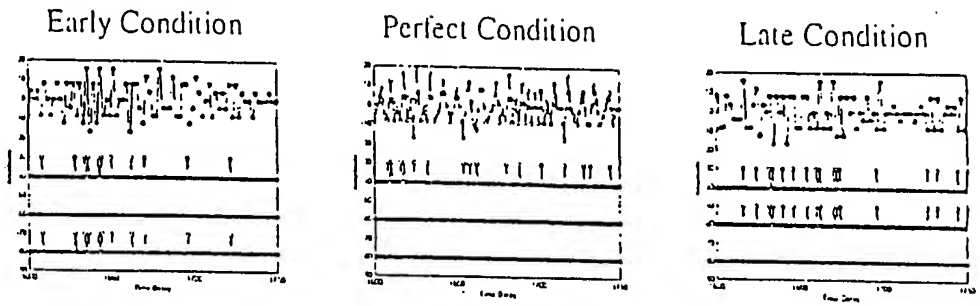
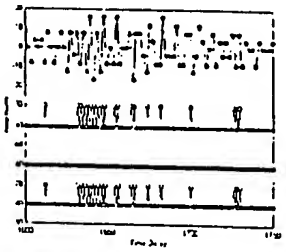


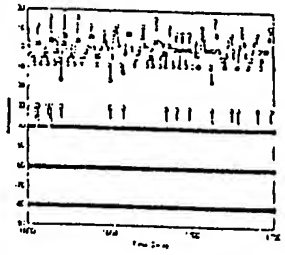
Figure 30

Waveform 1 : Sum of S_e and S_o of Figure 16, which constitutes the input to the modified transition detector.
Waveform 2 : The transition detection flag (F).
Waveform 3 : The synchronisation-late flag (L).
Waveform 4 : The synchronisation-early flag (E).

Early Condition



Perfect Condition



Late Condition

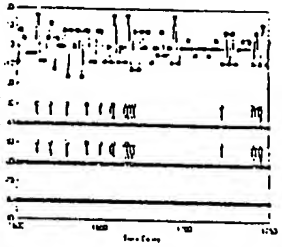


Figure 31

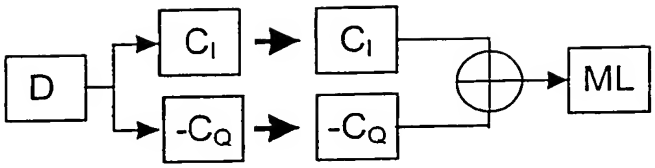
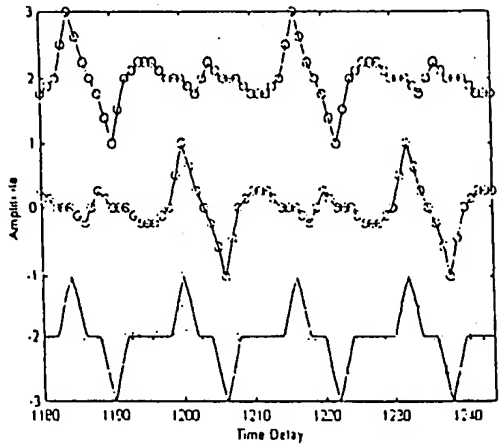


Figure 32



Waveform 1 : The correlation between the received signal and S_0.
Waveform 2 : The correlation between the received signal and S_2.
Waveform 3 : Sum of waveform 0 and 2.

Figure 33

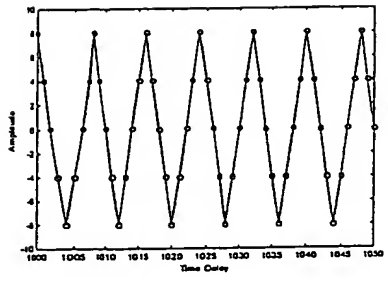

Amplitude
1000
1005
1010
1015
1020
1025
1030
1035
1040
1045
1050
Time Curve

Figure 34

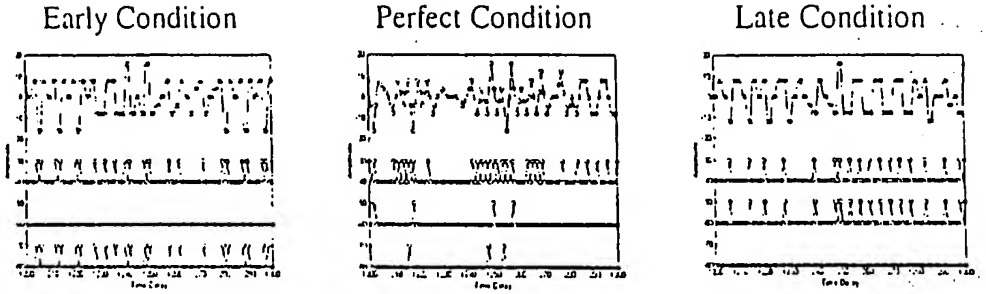
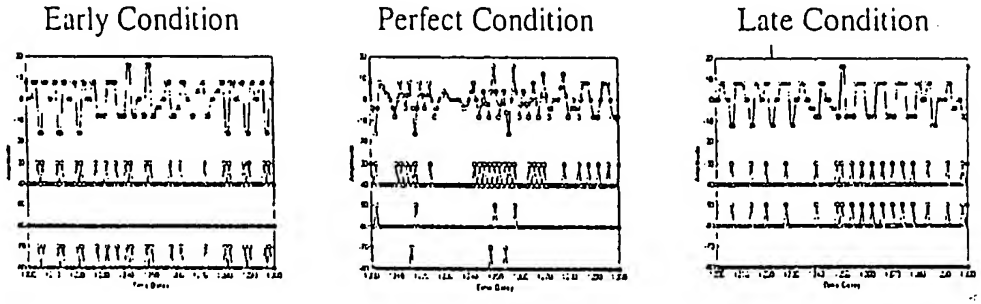


Figure 35



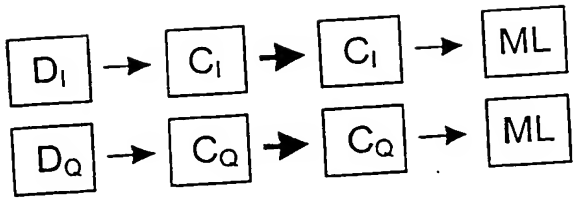
Waveform 1 : Sum of S_e and S_o of Figure 16, which constitutes the input to the modified transition detector.

Waveform 2 : The transition detection flag (F).

Waveform 3 : The synchronisation-late flag (L).

Waveform 4 : The synchronisation-early flag (E).

Figure 36



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